Patent Attorneys' Candidate Examination – Electronics
November 2017

Dear Examinee -

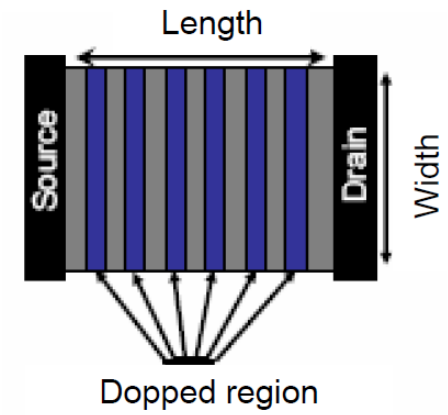
An inventor presents his invention to you and requests that you draft a patent application to protect the invention.

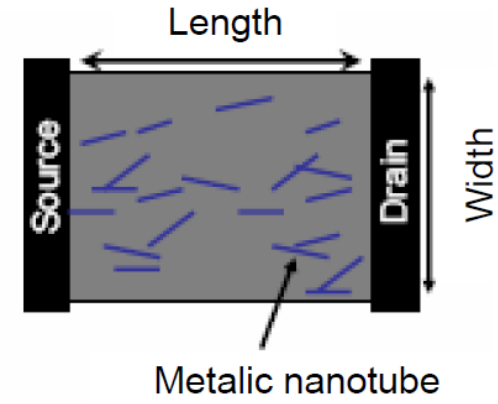
The invention as presented by the inventor:

My invention relates to a thin film transistor, which is a field effect transistor (FET), in which an electric field created by the gate controls the flow of current along the transistor channel from the source to the drain.

It is a common goal to increase the current through the transistor. It is known to achieve this in a standard lateral configuration transistor by effectively shortening the channel length by including highly conductive regions in the channel. Shortening the effective length that the charge needs to pass through in the semiconductor reduces the overall channel resistance and results in a higher current.

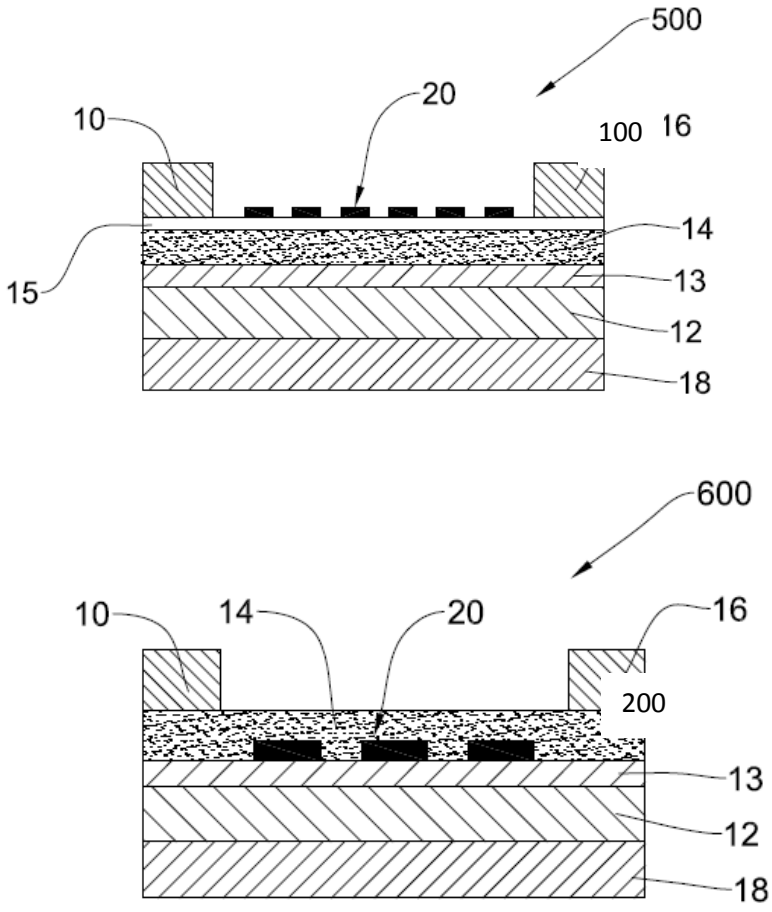
Such known configurations are for example as follows:





I suggest a novel transistor, which has significantly enhanced performance (higher currents and shorter switching times), while using the same materials and fabrication technology as state-of-the-art transistors, due to reduction of the effective length of the transistor channel without any doping of the channel material.

I prepared schematic figures showing two examples of the layout of transistors 100 and 200 demonstrating the main idea of my invention:



Here:

18 – substrate layer (e.g. SiO2);

12 - gate electrode;

13 - insulator layer;

14 - channel layer (e.g. semiconductor or polymer);

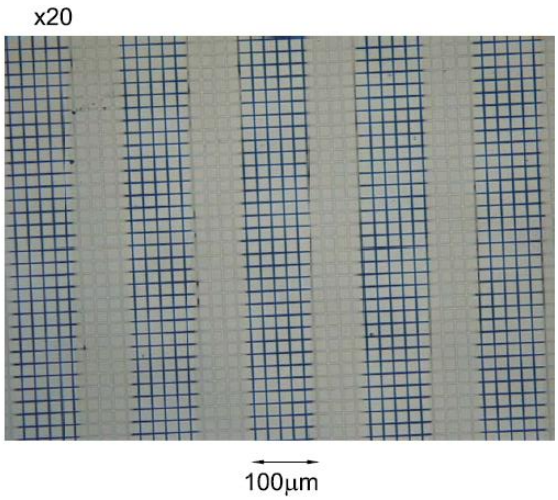
20 - patterned electrically conductive layer (**this is my invention**), e.g. metal islands spaced from one another (spacing between the islands varies across the patterned region such that length-dependent effects would be minimized and/or averaged out);

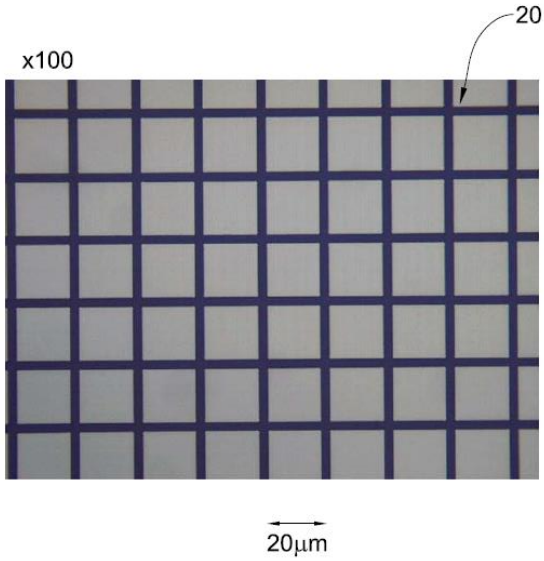
10 and 16 - source and drain electrodes;

15 – optional thin insulator layer, e.g. a block copolymer (this optimizes the current injection from the islands into the channel).

These two examples show that patterned electrically conductive layer 20 may be located above or below the channel layer 14.

The array of metal islands may be one- or two-dimensional (two-dimensional is preferred in order to prevent effects of local defects onto the entire structure):

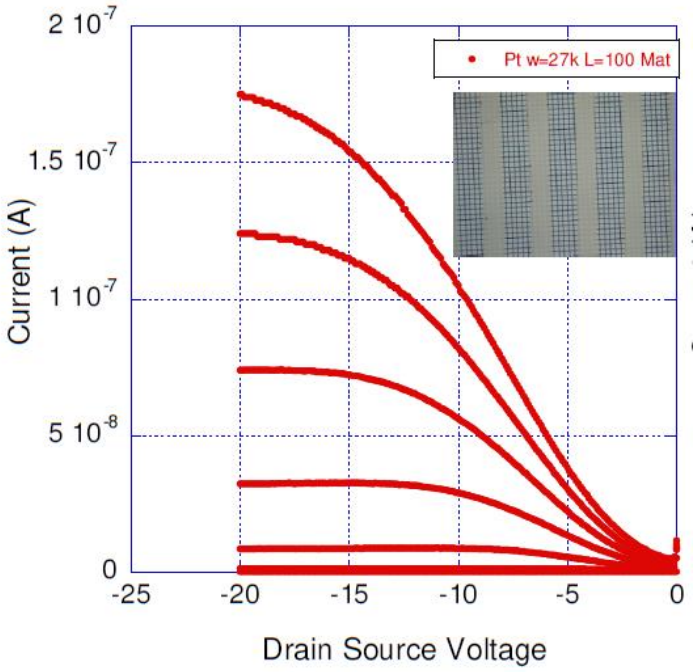




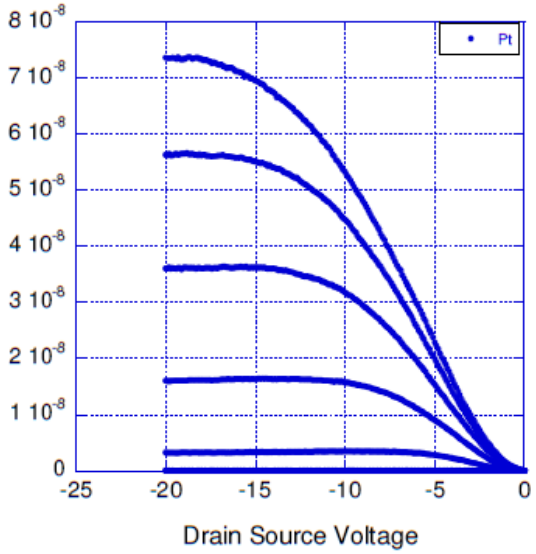
The patterned layer 20 can be achieved through the use of appropriate organic materials (preferably block copolymers) due to their varying affinity to metal atoms and/or conducting polymers. Some other methods include various printing, soft lithography techniques, or standard lithography.

I have experimentally demonstrated that my invention improves the FET performance (the electric current through the transistor as a function of drain/source voltage) as compared with that of the known FET structure.

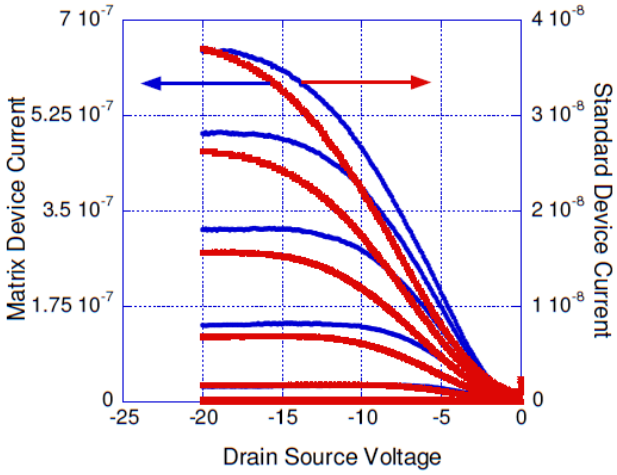
In the experiment, I used the experimental FET structure with a matrix of 27000μm width and 100μm length. The results for "my FET" are as follows:



The results for the standard FET using a matrix of 10000μm width and 5μm length are:



Here is the normalize current to the width/length ratio:



The results showed 16 times enhancement!!!, as compared to the conventional transistor.

Thin film transistor (TFT) of my invention can be used in various electronic devices. For example, it can be implemented as a light-sensitive switchable organic TFT (OTFT). Illumination can enhance the OTFT current by three orders of magnitude, while the device on/off state is controlled by the gate electrode. The light sensitive switchable OTFT may be used for large area sensor array as a full-page tablet scanner or as digital X-Ray plates.

By employing my invention, i.e. the patterned electrically conductive layer (non-continuous electrically-conductive film, e.g. metallic film or conducting polymer film) above or below the channel, the conductance of the channel is enhanced and the effect of the contacts is dramatically enhanced making the device "useful". In such pattern, higher electrically conductive regions (e.g. islands) are spaced by relatively low conductivity regions (e.g. dielectric, semiconducting regions).

*** End of the Disclosure of the Invention ***

Your tasks:

General direction: You are requested to present an initial full-draft of a patent application for the invention. The draft should include some background in the field to which the invention relates in order to indicate some general goals / problems known in the field (the inventor supplied some information); description of the invention; and claims.

If you find that certain details are missing or some aspects/features of the invention as described by you need some clarification / verification by the inventor – indicate what are these details and what aspects of the description you expect the inventor to complete / clarify. If you find these details essential for the drafting – assume what the details are (explain your assumption) and proceed based on these assumed details.

Score:

1. Draft patent application based on the description of the inventor - 35%
2. Draft at least 5 device and/or method claims in US style - 40%;
3. Draft the same claims in EP style (using two-part form), and if you believe that there is no need to reformulate the US-style claim into EP style, then please explain why - 15%
4. Please explain what defines the broadest scope of coverage of the patent? And what are dependent claims for? - 5%;
5. Whether and why it is recommended to draft both device and method claims? - 5%.

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