תרגום מאנגלית לעברית – אלקטרוניקה

נבחן יקר,

נא לתרגם את הטקסט הבא.

This method of the present invention provides the advantage of reduced off-chip delay by performing the selection between the component output signal and the test result signal prior to the clocking of the output stage by a transition of the clock signal of the electronic component. When the clock signal transitions, the component output signal is outputted by the output stage and does not have to pass through a multiplexer which selects the component output signal rather than the test result signal. As stated earlier, the critical time for determining the off-chip delay is the time period from the transition of the clock signal of the component until the component output signal appears at the output of the component. Since the selection between the component output signal and the test signal is performed prior to the clock transition, the component output signal does not pass through the multiplexer after the clock transition, thereby reducing off-chip delay.